Letters

An Optimized Three-Phase Multilevel Inverter Topology With Separate Level and Phase Sequence Generation Part

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***Abstract*—This paper presents an optimized, 3-ϕ, multilevel inverter (MLI) topology. The proposed system is derived by cascading the level generation part with the phase sequence generation part. Further, it can be operated at any required level depending upon the configuration of the level generation part. Thus, for higher level operation extra components are required at the level generation part only. Therefore, number of components required for the proposed MLI is lower than the conventional 3-ϕ MLI topologies for higher level operation. Further, the level generation part is shared by the three phases equally. This eliminates the possibility of phase unbalance. The working principle and the operation of the proposed MLI are supported with the simulation and experimental validations. Further, the proposed optimized MLI is also compared with theconventional 3-ϕ MLIs to prove its advantage.**

***Index Terms*—Common mode voltage, multilevel inverter, new topology, 3-ϕ.**

I. Introduction

OVER a few decades, multilevel inverters (MLIs) are at the focal point of continuing research due to the features of improved power quality, reduced total harmonic distortion, high modularity, minimum filter requirement, reduced switching loss, low dv/dt stress, etc., [1]. In literature, the authors have proposed multitude of the 1-ϕ and 3-ϕ, MLI configurations with respect to the component minimization and level maximization [2]. The most common technique adopted in the 1-ϕ systems is the separation of polarity and level generation parts [2]. However, this technique is yet to be applied in the 3-ϕ MLIs for the reduction and increment in the number of components and levels, respectively.

It is well known that in case of conventional 3-ϕ, MLI solutions such as neutral point clamped (NPC) and flying capacitor (FC), the number of components is quite high. Further, it increases in the multiple of three with the increment in the number of levels [3], [4]. This makes the NPC and FC MLIs expensive for their higher level operation. Further, the capacitor voltage balancing becomes a challenging task for more than 3-level operation. Most of these issues are addressed by the cascaded MLIs (CMLIs) [5]–[8] employing isolated dc voltage sources with an asymmetrical configuration [9]. Asymmetrical configuration helps to achieve more number of levels at the output with reduced number of components [2]. However, the dc voltage sources in the CMLIs are not equally shared by the three phases. This may introduce an unbalance in the 3-ϕ output of the CMLI [10]. Apart from this, the number of the isolated dc voltage sources required is also high for the CMLI configurations.

To address the above-mentioned issues, a new optimized 3-ϕ MLI configuration is proposed in thispaper. The proposed 3-ϕ MLI is derived by using the concept of level and polarity generation, as used in the case of 1-ϕ MLIs [11]. However, the task of polarity generation part is executed by the phase sequence generation part in the proposed 3-ϕ, MLI. Usage of separate level and phase sequence generation parts helps in reducing the number of components significantly in the proposed system. Also, for a higher level operation of the proposed MLI, the modification is required at the level generation part only. Thus, the number of extra components required for the higher level operation is reduced and is less than the multiple of three. Further, the proposed MLI can also be operated in asymmetrical configuration. This will further help in maximizing the number of levels at the output. Moreover, the level generation part is common to all the three phases. This eliminates the probability of an unbalance in the 3-ϕ output.

Rest of the paper consists of four more sections. Working principle of the proposed topology is given in Section II. Simulation and experimental results are shown and explained in Sections III and IV, respectively. And concluding declarations are given in Section V.

II. Working Principle of Proposed Topology

The circuit diagram of the proposed optimized MLI configuration for *m*-level operation is shown in Fig. 1. It consists of two parts, (i) level generation part (LGP) and (ii) phase sequence generation part (PSGP). The LGP is realized using two identical basic units (BUs) connected in series, as can be seen in Fig. 1(a). BUs used in LGP consists of "*n*" number of series connected subunits or cells with a dc voltage source, as given in

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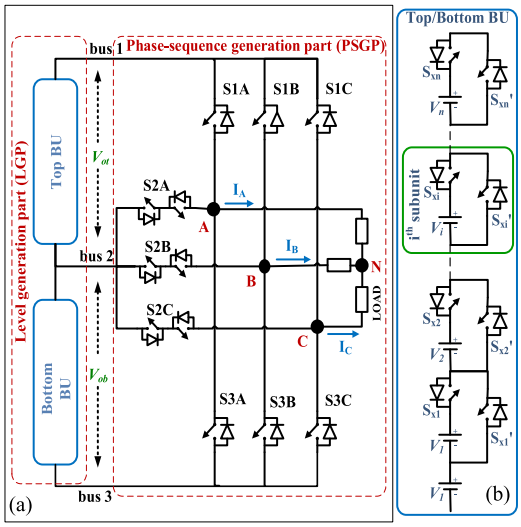

Fig. 1. (a) Circuit schematic for the proposed *m*-level MLI. (b) Configuration of top/bottom BU.

Fig. 1(b). Each subunit/cell again consists of dc voltage source and a pair of complementary switches.

For, e.g., the *i*th subunit/cell contains a dc voltage source with the magnitude $V_{\rm i}$ and a pair of complementary power switches, $S_{\rm xi}$ and $S_{\rm xi}$' [where, $x = 1$ for top BU and $x = 2$ for bottom BU and $i \in (1, 2, \ldots, n)$]. Thus, for the realization of complete LGP, the total numbers of the switches and sources required are "4n" and "$2(n + 1)$," respectively. The advantages of having multiple dc sources are improved reliability, power extraction capability [12], and capacitor voltage balancing capability [3]. These isolated dc sources can be realized using multi-winding transformer followed by multiple diode bridge rectifiers [8] or solar PV sources [6]. Discontinuity in the input current of the PV source can be taken care of by connecting a buffer capacitor across the PV source and suitable PWM strategy [13].

Further, it can be observed from Fig. 1 that the LGP has three output buses/terminals which are referred as bus 1, 2, and 3. The top BU of LGP is connected between buses 1 and 2, whereas the bottom BU is connected between buses 2 and 3. These three buses are also the common link between LGP and PSPG. The PSGP consists of a T-type inverter with three input and output terminals. The input terminals are directly connected to three buses 1, 2, and 3. And the output terminals are connected to 3-ϕ, *Y*-connected load. Thus, any phase *P* can be connected to bus *Q* (where $P \in (A, B, C)$ and $Q \in (1, 2, 3)$) using power switch SQP. Further, the switches connecting bus 1 and 3, i.e., S1P and S3P are realized with single MOSFETs. And the switch S2P is realized using the antiseries connection of two MOSFETs as indicated in Fig. 1(a). Thus, PSGP is realized using 12 MOSFETs, which remains fixed for any level operation of the proposed MLI.

Therefore, the total number of the switches "NSW" required for the realization of proposed MLI with "*n*" number of subunits in each BU is given by

$$N_{\rm SW} = 4n + 12. \tag{1}$$

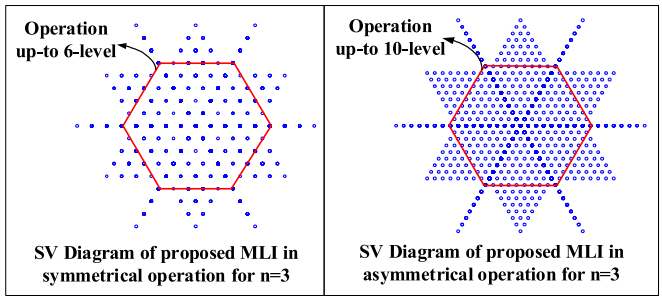

Fig. 2. SV diagram of proposed MLI in (a) symmetrical operation and (b) asymmetrical operation for $n = 3$.

Similarly, the total number of dc voltage sources "$N_{\rm SRC}$" required by the proposed MLI is given by

$$N_{\rm SRC} = 2(n + 1). \tag{2}$$

Now with the increasing value of "*n*", the number of voltage levels at the output will increase and it also depends upon the magnitudes of the dc voltage sources. Depending upon the magnitudes of the dc voltage sources, the proposed MLI can have two types of configurations, as described in the following sections.

A. Symmetrical Configuration

In this configuration, all dc voltage sources have equal magnitude, i.e.,

$$V_i = V_{\rm dc}. \tag{3}$$

In the case of symmetrical configuration, the maximum number of levels "$N_{\rm LS}$" generated by the proposed MLI is given as

$$N_{\rm LS} = n + 3. \tag{4}$$

The advantage of symmetrical configuration is that it has huge number of redundant states, which increases exponentially with the number of levels.

B. Asymmetrical Configuration

In this configuration, the magnitude of the dc voltage source in *i*th subunit is given by

$$V_i = 2^{i-1} V_{\rm dc}. \tag{5}$$

Further, the maximum number of levels, "N_{LA}" generated by the MLI in case of asymmetrical configuration is given as

$$N_{LA} = 2^n + 2. \tag{6}$$

To justify the number of levels, the space vector (SV) diagram of the proposed inverter with $n = 3$ for both symmetrical and asymmetrical configurations is shown in Fig. 2. The thick red line in Fig. 2 shows the operating boundary of the proposed MLI. Even if the vectors outside the operating boundary are not considered, the proposed MLI still is advantageous when compared to conventional MLI topologies such as NPC, FC, and CHB MLI. A graph is plotted between the number of levels and power semiconductor switches for both conventional

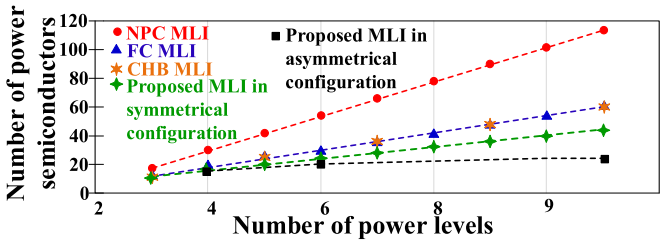

Fig. 3. Plot between the number of switches versus number of levels for the proposed topology and the conventional MLI topologies.

TABLE I
COMPARISON OF THE PROPOSED TOPOLOGY WITH NPC MLI FOR FOUR-LEVEL OPERATION

Parameters	Proposed MLI	NPC MLI
Total voltage rating of the switches	11.34 Vdc	12 Vdc
Number of controlled switches	16	18
Number of clamping diodes	0	18
Driver circuit requirement	16	18
Number of switches conducting	6	9
Efficiency	97.79%	95.55%

The comparison is done assuming both MLIs produce maximum +Vdc line-to-line voltage with four-level operation.

MLI and proposed MLI configurations (symmetrical and asymmetrical) in Fig. 3. It can be observed from Fig. 3 that the proposed configuration can realize more number of levels with reduced number of switches in both symmetrical and asymmetrical configurations. The proposed MLI is also compared with the conventional NPC MLI for four-level operation, as given in Table I. It can be observed from Table I that the proposed MLI requires reduced number of switches and driver circuits for its four-level operation. The total voltage rating of the devices is also less for the proposed MLI. Reduced number of conducting switches results in reduced conduction loss compared to NPC MLI. Similarly, reduced requirement of driver circuit reduces the driver circuit loss and cost for the proposed MLI as compared to the NPC MLI. Apart from this, the proposed MLI has higher efficiency than NPC for four-level operation, as can be seen from Table I. (The efficiency calculations are done considering both systems to be of 4.67 kW rating and driven at 25 kHz switching frequency with the loss calculation methods given in [14]. The IGBT and diode models are also used from [14]. Loss calculations were done for both NPC and the proposed MLI.)

III. Simulation Results

The performance of the proposed 3-ϕ, MLI has been analyzed with the help of a simulation model, developed in MATLAB/Simulink software integrated with PLECS block-set. Specifications and values of the parameters used in the simulation of the proposed system are summarized in Table II for three subunits ($n = 3$). Simulation results are given for both symmetrical and asymmetrical operation in the following sections.

TABLE II
SIMULATION PARAMETER SUMMERY

Parameter	Value
Output voltage frequency	50 Hz
Switching frequency	5 kHz
V_{dc}	100 V
Per phase load resistance	185 Ω
Per phase load inductance	0.01 H
Amplitude modulation index	1
Number of subunits (n)	3

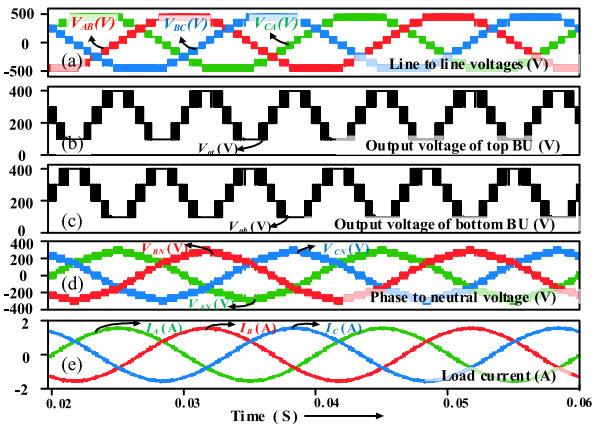

Fig. 4. Simulation results showing (a) line-to-line voltages, (b) output voltage of top BU, (c) output voltage of bottom BU, (d) phase-to-neutral voltages and (e) load current waveforms of the proposed 3-ϕ MLI in symmetrical operation.

A. Symmetrical Configuration

According to (4) and Fig. 2(a), the proposed MLI operates at 6-level in a symmetrical configuration for $n = 3$. This can be justified from the simulation results showing the line-to-line voltage waveform in Fig. 4(a) for symmetrical configuration of the proposed MLI. Further, the output voltages of top and bottom BUs, "V_{ot}" and "V_{ob}" (Fig. 1), respectively, are also shown in Fig. 4(b) and (c). It can be observed that four voltage levels are present in the waveforms of "V_{ot}" and "V_{ob}." Therefore, the operation in symmetrical configuration using three subunits in each BU is also supported by the simulation results. Moreover, the simulated three phase-to-neutral voltages and load currents are also shown in Fig. 4(d) and (e), respectively.

B. Asymmetrical Configuration

The proposed MLI is also simulated for asymmetrical configuration with $n = 3$. In this condition, the proposed MLI operates at 10-level, according to (5) and Fig. 2(b). This is also supported by the simulated line-to-line voltage waveforms as shown in Fig. 5(a). Further, for asymmetrical configuration the output voltages of top and bottom BUs are presented in Fig. 5(b) and (c). The presence of eight voltage levels in the waveforms of "V_{ot}" and "V_{ob}" supports the operation of the proposed MLI in asymmetrical configuration. Further, the simulation results showing phase-to-neutral voltages and load currents are presented in Fig. 5(d) and (e). It can be seen from Fig. 5(e) that

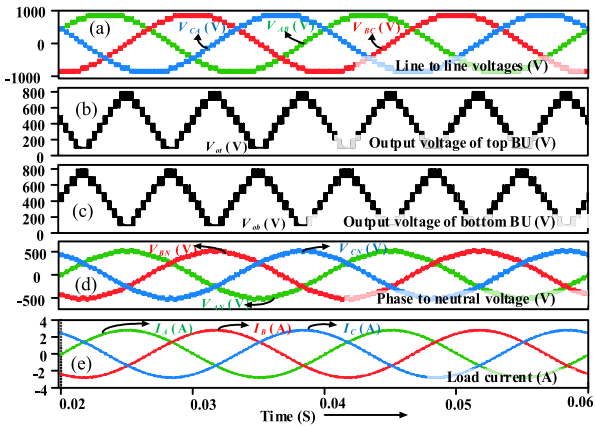

Fig. 5. Simulation results showing (a) line-to-line &&voltages, (b) output voltage of top BU, (c) output voltage of bottom BU, (d) phase-to-neutral voltages and (e) load current waveforms of the proposed 3-ϕ MLI in asymmetrical operation.

TABLE III
LABORATORY PROTOTYPE PARAMETER SUMMERY

Parameter	Value
Output voltage frequency	50 Hz
Switching frequency	2 kHz
V_{dc}	20 V
Per phase load resistance	185 Ω
Per phase load inductance	0.01 H
Amplitude modulation index	1
MOSFET	IRF840
Controller	TMS320LF28069
Data acquisition	Tektronix DPO 3034
Number of subunits (n)	1

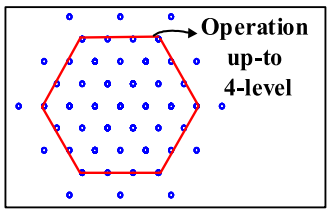

Fig. 6. SV diagram of proposed MLI for $n = 1$.

the load currents become more "ripple free" in a asymmetrical configuration than a symmetrical configuration.

IV. Experimental Results

A laboratory prototype of the proposed optimized system is fabricated to verify its performance. The system parameters taken for the laboratory prototype are given in Table III. As can be seen from Table II that the number of subunits for the fabricated prototype is taken as 1 ($n = 1$). The SV diagram of the MLI prototype for $n = 1$ is shown in Fig. 6. The thick red line denotes the four-level operating boundary of the proposed MLI. It can be observed that the MLI prototype will generate four-level output for both symmetrical and asymmetrical operation as $n = 1$. This can also be obtained by putting $n = 1$ in (4) and (6).

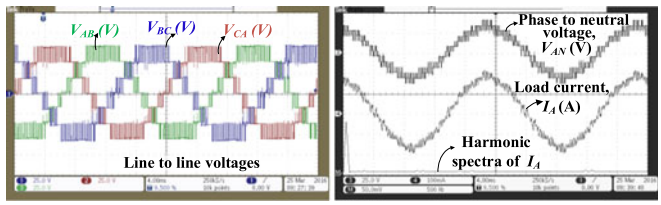

Fig. 7. Experimental results showing (a) line-to-line voltage (b) phase-to-neutral voltage, load current and harmonic spectra of the load current of the proposed MLI.

By operating the proposed MLI in the SV hexagon inside the red line from Fig. 6, three line-to-line voltages can be generated at the inverter output. These line-to-line voltage waveforms are shown in Fig. 7(a). It can be observed that each line-to-line voltage waveform has seven levels including the positive and negative polarity. This justifies the four-level operation of the proposed MLI.

Fig. 7(b) shows the phase-to-neutral voltage, load current and the harmonic spectra of the load current. It can be observed from Fig. 7(b) that the phase-to-neutral voltage waveform contains 13 discrete voltage levels. This is another justification of the four-level operation of the proposed MLI. Further, the harmonic spectra of load current contain almost negligible harmonics with respect to the fundamental. This will ensure better power quality performance of the proposed MLI.

V. Conclusion

This paper presents an optimized 3-ϕ MLI configuration with reduced number of component. The prominent features of the proposed MLI are as follows.

1) The proposed MLI configuration is built by cascading LGP and PSGP.
2) For higher level operation, only switches required are at the BUs only, which resides in the LGP. This reduces the requirement of extra devices compared to conventional topologies.
3) Also, each dc voltage source in the presented MLI topology is equally shared by all the phases. Thus, any chance of inter-phase asymmetry is avoided.

The above-mentioned points support that the proposed MLI is an optimized configuration for 3-ϕ operation with reduced number of switches. However, the proposed configuration is operated by using the SVs up to the red line only. The further work with an improved PWM strategy, which takes all the SVs in account, will be presented in the regular paper. This will further increase the number of levels at the output and linearity can be maintained in the overmodulation region with improved dc-bus utilization.

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